UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,743	05/01/2006	Heinz-Werner Morrell	502901-218PUS	7809

27799 7590 05/04/2007

COHEN, PONTANI, LIEBERMAN & PAVANE
551 FIFTH AVENUE
SUITE 1210
NEW YORK, NY 10176

EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

MAIL DATE	DELIVERY MODE
05/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,743	MORRELL ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12-14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2004/0002808 to Hashimoto et al. in view of U.S. Patent No. 4,727,549 to Tulpule et al.

With respect to claim 12, Hashimoto discloses a safety device for a rotation rate sensor (0087, lines 1-3), comprising a sensor element (0087, lines 1-3 and "130" (Figure 3) and circuits including a function section (i.e. sensor interface "111a") (0093, lines 1-3 Figure 1), a checking section (i.e. microprocessor "110") (0101, lines

1-6) and a monitoring section (0105, lines 1-8), the function section including functional components supporting the function of the sensor element and producing a sensor output signal (0087, lines 1-3, 0093, lines 1-3, and 0132, lines 1-4), the checking section including checking components designed for the continuous checking of the functional components (0237, lines 1-9), and the monitoring section comprising monitoring components designed for monitoring the checking components at least once during one operating cycle (0105, lines 1-8), the monitoring components comprising a clock detector component monitoring a clock (i.e. WD) of a microcomputer contained in the checking section and a watchdog circuit monitoring the microcomputer (0105, lines 1-8).

With respect to claim 13, Hashimoto discloses that the checking components measure values in the function section and compare the measured values with limit values (0237, lines 1-9).

With respect to claim 14, Hashimoto discloses that the checking components measure the sensor output signal and compare the measured sensor output signal with limit values (0237, lines 1-9).

With respect to claim 18, Hashimoto discloses that the monitoring components are designed essentially to monitor digital checking components (i.e. the microprocessor of the checking components) (0105, lines 1-8).

As noted above, the invention of Hashimoto teaches many of the features of the claimed invention and while the invention of Hashimoto does teach a watchdog circuit as part of a monitoring section for monitoring the microcomputer of the

checking section, Hashimoto does not specifically disclose a memory testing device for testing memories within the checking section.

Tulpule teaches a watchdog activity monitor for use with a high coverage processor self-test comprising a microprocessor (column 6, lines 35-44) which is tested (column 6, lines 45-51) using an independent (column 2, lines 15-23) watchdog circuit (column 7, lines 3-14) that tests the memories of the microprocessor (column 7, lines 24-40).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hashimoto to specifically disclose means for testing memories within the checking section, as taught by Tulpule, because, as suggested by Tulpule, the combination would have improved the monitoring of Hashimoto by confirming that the microprocessor address decoding is accurate thereby confirming overall operation of the microprocessor of Hashimoto and insuring accurate sensor functionality (column 7, lines 36-53).

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. in view of Tulpule et al. and further in view of U.S. Patent No. 4,916,698 to McCann.

As noted above, the invention of Hashimoto and Tulpule teaches many of the features of the claimed invention and while the invention of Hashimoto and Tulpule does teach interface/conditioning circuitry as part of the functional components of the function section and checking components, including a microprocessor,

designed for continuous checking of the functional components, the combination does not specify that the checking components comprise a test injector producing and supplying test signals to the functional components, the checking components testing the functional components and measuring a reaction of the functional components to the test signals.

McCann teaches a failure detection mechanism for microcontroller based control system comprising a speed sensor and signal conditioning circuitry acting as part of functional components (column 2, lines 25-31 and 38-41) and a microprocessor acting as part of a checking section that comprises a test injector producing and supplying test signals to the functional components, the checking components testing the functional components and measuring a reaction of the functional components to the test signals (column 3, lines 5-13).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hashimoto and Tulpule to specify that the checking components comprise a test injector producing and supplying test signals to the functional components, the checking components testing the functional components and measuring a reaction of the functional components to the test signals, as taught by McCann, because, as suggested by McCann, the combination would have improved sensing system of Hashimoto and Tulpule by insuring that the various input/output ports of the sensor and interface/conditioning circuitry of Hashimoto and Tulpule are appropriately responding to the microprocessor (column 3, lines 5-13).

5. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. in view of Tulpule et al. and further in view of U.S. Patent No. 5,406,485 to Wise et al.

As noted above, the invention of Hashimoto and Tulpule teaches many of the features of the claimed invention and while the invention of Hashimoto and Tulpule does teach obtaining data from functional components that are part of a function section of a vehicle rotation rate sensor as well as a checking section for accessing the output of the functional components, the combination does not explicitly indicate that the function section comprises digital components and analog components, the checking components including checking analog components and at least one ADC for accessing registers of the digital components and measuring analog signals at the analog components.

Wise teaches a method and apparatus for detecting faulty operation of a wheel speed sensor comprising a sensor (column 3, lines 11-13) and associated interface and functional components (i.e. function section) (column 3, lines 11-20) wherein the function section comprises digital components (column 3, lines 51-54) and analog components (column 4, lines 39-57), and checking components include checking analog components for measuring analog signals at the analog components (column 3, lines 42-46) and at least one ADC for accessing registers of the digital components (column 3, lines 51-60).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hashimoto and Tulpule to explicitly indicate that the function section

comprises digital components and analog components, the checking components including checking analog components and at least one ADC for accessing registers of the digital components and measuring analog signals at the analog components, as taught by Wise, because the invention of Hashimoto and Tulpule discloses a system for monitoring the output of a plurality of vehicle sensors (Hashimoto; Figure 1) and Wise suggests an applicable vehicle sensor and associated monitoring method that would have provided corresponding means for insuring the accuracy of the speed sensor while providing increased functionality of Hashimoto and Tulpule by including advanced conditioning aspects and the ability to store the data for speed computations (column 2, lines 33-46 and column 3, lines 42-46 and 51-60).

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. in view of Tulpule et al. and further in view of U.S. Patent No. 6,568,267 to Chida et al.

As noted above, the invention of Hashimoto and Tulpule teaches many of the features of the claimed invention and while the invention of Hashimoto and Tulpule does teach a function section, checking section, and monitoring section, the combination does not specifically indicate that the sections are formed by an ASIC with dedication sections.

Chida teaches a sensing devices and sensor apparatus wherein the sensor is formed from an ASIC, inherently comprising gates, having a main central processing

section and separate dedicated sections for performing different specific computations, functions, and other processes (column 20, lines 57-65).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hashimoto and Tulpule to specifically indicate that the sections are formed by an ASIC with dedication sections, as taught by Chida, because Chida suggests that, and as is known by one having ordinary skill in the art, ASICs with dedicated functionality are a common device for providing different dedicated functional sections as would be desirable in the sensor system of Hashimoto and Tulpule (column 20, lines 57-65).

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. in view of Tulpule et al. and further in view of U.S. Patent No. 6,366,005 to Ishikawa et al.

As noted above, the invention of Hashimoto and Tulpule teaches many of the features of the claimed invention and while the invention of Hashimoto and Tulpule does teach a safety device for a rotation rate sensor (Hashimoto; 0087, lines 1-3), the combination is silent as to the specific makeup of the rotation rate sensor.

Ishikawa teaches a tuning fork type vibration gyro acting as a rotation rate sensor generating an analog output signal to an analog-to-digital converter (column 11, lines 35-60).

It would have been obvious to one having ordinary skill in the art to modify the invention of Hashimoto and Tulpule to specify that the sensor is a vibration gyro

generating an analog output signal, as taught by Ishikawa, because the invention of Hashimoto and Tulpule is silent as to the specific makeup of the rotation rate sensor and Ishikawa teaches a combination that would have provided a well known, accurate means for implementing the rotation rate sensor thereby improving the applicability of the system of Hashimoto and Tulpule by employing a conventional sensor that is capable of preventing destruction of a tuning fork vibrator with improved accuracy through unnecessary signal compensation (column 1, lines 8-11 and column 3, lines 13-21).

Response to Arguments

8. Applicant's arguments filed April 16, 2007, have been fully considered but they are not persuasive.

Applicant argues:

> The Examiner alleges that paragraph 0105, lines 1-8, of Hashimoto discloses the claimed monitoring section. However, that portion of Hashimoto discloses only that a watchdog timer circuit WDT 119 monitors a watchdog signal WD generated by a microprocessor and that the watchdog timer circuit WDT 119 generates a restart signal RST when the watchdog signal WD is abnormal. Accordingly, Hashimoto fails to teach or suggest that the monitoring section includes "a clock detector component", "a watchdog circuit monitoring the microcomputer", and "a memory testing device for testing memories within the checking section", as expressly recited in independent claim 12.
>
> Even if the watchdog timer circuit WDT 119 of Hashimoto is considered to be applicants' claimed "clock detector component" and/or the "watchdog circuit" (which applicant does not believe to be proper), the watchdog timer circuit WDT 119 of Hashimoto still fails to disclose, teach or suggest "a memory testing device for testing memories within the checking section".

The Examiner asserts that Hashimoto discloses:

> The watch dog signal WD of the microprocessor 110 is a pulse train generated by the microprocessor 110, and is given to a watch dog timer circuit (WDT) 119. This watch dog timer circuit 119 monitors the watch dog signal WD, and when a pulse width of the watch dog signal WD is abnormal, this circuit generates a reset output RST to restart the microprocessor 110, and sets the abnormality storage circuit element 116. (0105, lines 1-8).

This section of Hashimoto clearly discloses a clock detector component monitoring a clock (i.e. WD) of a microcomputer contained in the checking section and a watchdog circuit monitoring the microcomputer.

The Examiner asserts that Hashimoto is not relied upon for the teaching of "a memory testing device for testing memories within the checking section" as this feature is taught by Tulpule.

Applicant argues:

> Tulpule fails to teach or suggest what Hashimoto lacks. Tulpule disclose a watchdog activity monitor, but fails to teach or suggest a checking circuit or "a memory testing device for testing memories within the checking section", as recited in independent claim 12. In view of the above amendments and remarks, independent claim 12 is deemed allowable over the prior art of record.

The Examiner asserts that Tulpule discloses:

> The block diagram illustration of FIG. 2 is a functional model of a signal processor 50 including registers 52, ALU 54, program counter 56, control unit 58, interrupt control 60, and address/timing 61 functional blocks. Of course, the typical signal processor will also include other major functional blocks which are not included for the sake of simplicity. Each of the functional block may be conceptualized as communicating with a data bus 62, an address bus 64, and a control bus 65.
>
> FIG. 3 is an illustration of a comprehensive test procedure which may be carried out on a processor modeled according to the functions which it is capable of carrying out as, for example, in FIG. 2. Thus, the test procedure illustrated in FIG. 3 is designed for specific use on a typical signal processor. (column 6, lines 35-51).

> Each of the tests described below is designed to energize a small subset of instructions using prespecified data chosen to energize the maximum number of flipflops, gates, etc., involved in the execution of each particular instruction. The test results are compared with expected results and the next instruction test started on the successful completion of the previous test. However, if the test is not successful as indicated by the comparison, a branch to step 102 is made for sending an (early) ticket-punch signal to the WAM. This action being earlier than expected, trips the external WAM and leads to a channel sever.
>
> After starting the self-test, the processor performs a register test in step 104. The purpose of this test is to verify register address decoding for both bit and word modes. In addition, the register memory cells are checked for stuck bits. (column 7, lines 24-40).

Given the well-known definition of a register as a "memory device that is part of computer memory that has a specific address and that is used to hold information of a specific kind" and Hashimoto's teaching of a safety device for a rotation rate sensor comprising a checking section (i.e. microprocessor "110") (0101, lines 1-6), the Examiner asserts that the above-cited section of Tulpule does teach "a memory testing device for testing memories within the checking section".

The Examiner further asserts that it would have been obvious to one having ordinary skill in the art to modify the invention of Hashimoto to specifically disclose means for testing memories within the checking section, as taught by Tulpule, because, as suggested by Tulpule, the combination would have improved the monitoring of Hashimoto by confirming that the microprocessor address decoding is accurate thereby confirming overall operation of the microprocessor of Hashimoto and insuring accurate sensor functionality (column 7, lines 36-53).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent Application Publication No. 2003/0187569 to Iwagami et al. teaches a vehicle-mounted electronic control apparatus.

U.S. Patent No. 6,510,397 to Choe teaches a method and apparatus for self-diagnosis of a sensor.

U.S. Patent No. 5,890,078 to Furuta teaches a synthetic control system for an automobile.

U.S. Patent No. 5,791,432 to Fushimi et al. teaches a steering control apparatus for an automotive vehicle.

U.S. Patent No. 5,713,643 to Esselbrugge et al. teaches a control circuit for automotive vehicle motion control systems.

U.S. Patent No. 5,588,720 to Mattern teaches a circuit arrangement for a brake system with anti-lock system and/or traction control.

U.S. Patent No. 5,170,343 to Matsuda teaches a fail-safe system for multiple control systems having at least one common sensor for monitoring a common control parameter.

Webster's Online Dictionary, "Register", teaches the well-known definition of a register as a "memory device that is part of computer memory that has a specific address and that is used to hold information of a specific kind."

10. Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey R. West
Primary Examiner
Art Unit - 2857

April 29, 2007